IN THE SPECIFICATION

Replace the second paragraph of page 9 of the specification, with the following paragraph starting on line 7:

FIG. 5 illustrates a diagram 500 to control a plurality of delay compensation buffers DCB 1 through DCB 4. Referring to **FIG. 5**, IMA access device 410 is a sending end that transmits ATM cells of "A B C D" on links 430, which include links 1 through 4. IMA access device 450 is a receiving end that receives ATM cell "A" on link 1 in DCB 1, ATM cell "B" on link 2 in DCB 2, ATM cell "C" on link 3 in DCB 3, and ATM cell "D" on link 4 in DCB 4. IMA access device 450 also includes a DCB control mechanism 555 coupled to DCBs 1 through 4. DCB control mechanism 555 writes the ATM cells and reads the ATM cells to and from DCBs 1 through 4. To provide transparency of inverse multiplexing, DCB control mechanism 555 outputs the ATM cells in the same order that IMA access device 410 received them.

Replace the third paragraph of page 9 of the specification, with the following paragraph starting on line 17:

DCB control mechanism 555 implements a read pointer operation that circumvents the disadvantages of the prior art buffering schemes. For one embodiment, DCB control mechanism 555 controls a read pointer for DCBs 1 through 4 to move slightly faster than a write pointer for a link in the IMA group. That is, the cells are read out at a rate faster than they arrive into a DCB from links 430. For example, assume that cells arrive for each data link of the IMA group at every 276 microseconds. The write pointer of each link has to increment once every 276 microsecond.